In re Patent Application of:
ROCHE ET AL.
Serial No. **10/039,765**
Confirmation No. **9186**
Filed: **NOVEMBER 7, 2001**

In the Claims:

Claims 1-19 (Cancelled).

20. (Currently Amended) A method of transmitting data between a master device and a slave device via a clock line and at least one data line, the clock line being maintained by default on a first logic value, and each master and slave device being able to tie the clock line to a potential representing a second logic value opposite the first logic value, the method comprising:

~~providing each master and slave device with the ability to tie the clock line to a potential representing a second logic value opposite the first logic value;~~

~~tying the clock line to the second logic value, via the master and slave devices, after data is applied to the data line;~~

~~maintaining the tie to the clock line by a first device of the master and slave devices to which the data is sent while the first device has not read the data;~~

~~maintaining the data on the data line by a second device of the master and slave devices sending the data at least until an instant when the clock line is released by the second device to which the data is sent; and~~

~~wherein the master device ties the clock line to the second logic value after applying data to the data line when the master device is sending the data to the slave device, and~~

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~~wherein the slave device detects the second logic value on the clock line, then ties the clock line to the second logic value and reads the data, when the slave device is receiving the data from the master device; and~~

~~wherein the master device ties the clock line to the second logic value when the master device receives data from the slave device, and wherein the slave device detects the second logic value on the clock line, then ties the clock line to the second logic value, and applies the data to the data line, when the slave device is sending data to the master device.~~

when the master device is sending data to the slave device and the slave device is receiving the data from the master device, then

the master device applies data to the data line, then ties the clock line to the second logic value,

the slave device detects the second logic value on the clock line, then ties the clock line to the second logic value and reads the data,

the slave device maintains the tie to the clock line at the second logic value while the slave device has not read the data,

the slave releases the tie to the clock line at the second logic value when the slave device has read the data, and

the master device maintains the data on

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the data line at least until an instant when the clock line is released by the slave device,

the master device releases the data on the data line after the clock line is released by the slave device and by the master device; and

when the slave device is sending data to the master device and the master device is receiving the data from the slave device, then

the master device ties the clock line to the second logic value,

the slave device detects the second logic value on the clock line, then ties the clock line to the second logic value, and then or simultaneously applies the data to the data line,

the master device maintains the tie to the clock line at the second logic value while the master device has not read the data,

the master device release the tie to the clock line at the second logic value when the master device has read the data,

the slave device maintains the data on the data line at least until an instant when the clock line is released by the master device, and

the slave device releases the data on the data line after the clock line is released by the master device and the slave device.

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Claims 21-23 (Cancelled).

24. (Previously Presented) A method according to Claim 20, wherein a time period that the slave device has to release the clock line after receiving data, is independent of any action by the master device, as the master device does not send any new data while the slave device has not released the clock line.

Claims 25-27 (Cancelled).

28. (Previously Presented) A method according to Claim 20, wherein when the clock line has the first logic value, a time period that the master device has to tie the clock line to the second logic value is independent of any action by the slave device.

Claims 29-30 (Cancelled).

31. (Previously Presented) A method according to Claim 20, wherein the first logic value is 1 and the second logic value is 0.

Claims 32-47 (Cancelled).

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48. (Currently Amended) A synchronous data transmission system comprising:

a clock line;

a data line;

a master ~~data transmitting/receiving~~ device comprising

a clock line connection terminal connected to the clock line,

at least one data line connection terminal connected to the data line,

a circuit for tying the clock line to a potential representing a second logic value that is the opposite of a first logic value, and

a data sending unit for waiting for the clock line to have the first logic value, applying data to the data line, tying the clock line to the second logic value after the data is applied to the data line, then releasing the clock line, and maintaining the data on the data line at least until the clock line has the first logic value, when the data is to be sent; and

a slave ~~data transmitting/receiving~~ device comprising

a clock line connection terminal connected to the clock line,

at least one data line connection terminal connected to the data line,

a circuit for tying the clock line to the

potential representing the second logic value,

a detector for detecting a change from the first logic value to the second logic value on the clock line, tying the clock line to the second logic value, reading the data on the data line, and releasing the clock line, when the data is to be received; and

~~wherein said master device ties the clock line to the second logic value after applying data to the data line when said master device is sending the data to said slave device, and wherein said slave device detects the second logic value on the clock line, then ties the clock line to the second logic value and reads the data, when the slave device is receiving the data from said master device; and~~

~~wherein said master device ties the clock line to the second logic value when said master device receives data from said slave device, and wherein said slave device detects the second logic value on the clock line, then ties the clock line to the second logic value, and applies the data to the data line, when said slave device is sending data to said master device.~~

wherein when said master device is sending data to said slave device and said slave device is receiving the data from said master device, then

said master device applies data to the data line, then ties the clock line to the second logic

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value,

said slave device detects the second logic value on the clock line, then ties the clock line to the second logic value and reads the data,

said slave device maintains the tie to the clock line at the second logic value while said slave device has not read the data,

said slave releases the tie to the clock line at the second logic value when said slave device has read the data, and

said master device maintains the data on the data line at least until an instant when the clock line is released by said slave device,

said master device releases the data on the data line after the clock line is released by said slave device and by said master device; and

wherein when said slave device is sending data to said master device and said master device is receiving the data from said slave device, then

said master device ties the clock line to the second logic value,

said slave device detects the second logic value on the clock line, then ties the clock line to the second logic value, and then or simultaneously applies the data to the data line,

said master device maintains the tie to the

clock line at the second logic value while said master device has not read the data,

said master device release the tie to the clock line at the second logic value when said master device has read the data,

said slave device maintains the data on the data line at least until an instant when the clock line is released by said master device, and

said slave device releases the data on the data line after the clock line is released by said master device and said slave device.

49. (Previously Presented) A system according to Claim 48, wherein said master device further comprises a data receiving unit for waiting for the clock line to have the first logic value.

50. (Previously Presented) A system according to Claim 48, wherein said slave device further comprises a detector for detecting a change from the first logic value to the second logic value on the clock line.

Claims 51-52 (Cancelled).